WHAT IS CLAIMED IS:

1. An ESD protection structure for an integrated circuit comprising:

a semiconductor substrate of a first conductivity type;

a well region of a second conductivity type disposed in the semiconductor substrate;

a first region of the first conductivity type disposed in the well region on the semiconductor substrate;

a second region of the second conductivity type disposed in and on the semiconductor substrate and spaced apart from the first region; and

an electrical isolation region disposed in the semiconductor substrate between the first region and the second region.

2. The ESD protection structure of claim 1, wherein the first conductivity type is P-type and the second conductivity type is N-type.

3. The ESD protection structure of claim 2, wherein the maximum dopant concentration of the semiconductor substrate is less than the maximum dopant concentration of the first region and the maximum dopant concentration of the well region is less than the maximum dopant concentration of the second region.

4. The ESD protection structure of claim 3, wherein the dopant concentration of the semiconductor substrate is $5x10^{15}$ atoms/cm^3, the maximum dopant concentration of the well region is $2x10^{17}$ atoms/cm^3, the maximum dopant concentration of the first region is $5x10^{20}$ atoms/cm^3, and the maximum dopant concentration of the second region is $5x10^{20}$ atoms/cm^3.

5. The ESD protection structure of claim 1, wherein the electrical isolation region is a shallow trench isolation region.

6. The ESD protection structure of claim 1, wherein the semiconductor substrate comprises a P- epitaxial silicon layer.

7. The ESD protection structure of claim 6, wherein the P- epitaxial silicon layer has a dopant concentration no greater than $5x10^{15}$ atoms/cm^3.

8. The ESD protection structure of claim 1 configured between an input/output line of the integrated circuit and GND.

9. The ESD protection structure of claim 1 configured between a V_{DD} line of the integrated circuit and a differential amplifier of the integrated circuit.

10. The ESD protection structure of claim 1 further comprising a bottom contact to the semiconductor substrate.

11. An ESD protection structure for use with RF frequency integrated circuits comprising:

a P- epitaxial silicon semiconductor substrate;

an N- well region disposed in the semiconductor substrate;

a P+ first region disposed in the N-well region on the P- epitaxial silicon semiconductor substrate;

an N+ second region disposed in and on the P- epitaxial silicon semiconductor substrate and spaced apart from the P+ first region; and

an electrical isolation region disposed in the P- epitaxial silicon semiconductor substrate between the P+ first region and the N+ second region.